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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,295	07/09/2001	Tetsuya Yano	FUJR 18.797	8755

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EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	11

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,295	YANO ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,20 and 21* is/are allowed.

6)☒ Claim(s) *1,4-6,9-19,22 and23* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 7, 8, 20 and 21 are allowed.

2. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The indicated allowability of claims 1 and 6 is withdrawn in view of the newly discovered references to Robertson and Narayanan and to Smith. Rejections based on the newly cited references follow.

Drawings

4. Figures 14-17 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheets should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1, 2, 4, 5, 11 and 23 are objected to because of the following informalities:

In claim 1: in line 7, "if number of times" is elliptical and apparently should be "if the number of times".

In claim 2: "the set value" apparently should be "a set value", as a different number from "said set number of times" should apparently be referred to.

In claim 4: in order to avoid needless confusion created by referring to the disclosed "DEC1" as performing a "second decoding processing" and referring to the disclosed "DEC2" as performing a "first decoding processing", "yb" in lines 7 and 11 apparently should be "yc", and "yc" in lines 7 and 9 apparently should be "yb".

In claim 5: similarly to the suggested changes to claim 4, "yb" in lines 7, 10 and 14 apparently should be "yc", and "yc" in lines 7, 9 and 13 apparently should be "yb".

In claim 11: "alternatively" apparently should be "alternately".

In claim 23: "units of turbo code consisted of a plurality of information block" is apparently prolix and should read as "turbo code".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 4, 6, 16-19 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,304,995 to Smith *et al* (hereafter Smith).

Smith discloses a turbo decoder (Fig. 3) including a constituent decoder (SISO2) providing a "first elementary decoder" that performs a "first decoding processing", a constituent decoder (SISO1) providing a "second elementary decoder" that performs a "second decoding processing", an "interleaving unit" (311), and a "deinterleaving unit" (320). It is here noted that the written disclosure of Smith indicates that decision unit (326) input should be shown coming from the adder (324) instead of the delay (322). Final results of decoding from both decoders contributes to the final output, via the adder (324), and the decoded output contributed by the "first elementary decoder" (SISO1) is output to the adder without an interleaving or deinterleaving step, and hence "directly without intervention of interleaving or deinterleaving".

Regarding claim 6, Smith limits the number of iterations (col. 6, line 50), and the means for selecting the outputs of the Nth iteration indicate a "selection circuit for selecting and outputting the results of first and second decoding processing ... wherein the nature of an error pattern in decoded data finally output is controlled by selecting", as the error pattern presumably changes from one iteration to the next.

Regarding claim 16, in Smith's decoder the output of SISO1 to the adder ((324) is not interleaved or deinterleaved, thereby indicating an "output means for outputting the results of decoding processing in the decoder directly without intervention of interleaving or deinterleaving".

Regarding claims 17-19 and 22, Smith's means for selecting the output of the Nth iteration provides a providing a "controller" or "selector" for outputting "one of the results of the first and second decoding processing", as each iteration creates another set of "results of the first and second decoding processing".

8. Claims 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,192,503 to Chennakeshu *et al* (hereafter Chennakeshu).

Referring to the iterative decoder shown by Chennakeshu in Fig. 5, an error detector (254) and a first decoder (252a) receive decoded output (253b) from a second decoder (252b) in parallel, and there is no suggestion in Chennakeshu of pausing the operation of either the error detector (254) or the first decoder (252a). Absent such pausing, processing of the second decoder output (253b) by the error detector (254) and by the first decoder (252a) presumably takes place without delay, and thus there is "detecting errors in results of previous decoding in parallel with a current decoding operation in the iterative decoding processing".

Further regarding claim 10, Chennakeshu's Fig. 5 decoding system apparently outputs "results of decoding" regardless of some "set number of times", and thus apparently further involves a "controller" for "halting the decoding operation" once decoding has been completed.

9. Claims 11, 14 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,233,709 to Zhang *et al* (hereafter Zhang).

Regarding claim 11, Zhang discloses a turbo decoder (Fig. 1) including a second constituent decoder (112) that performs a "first decoding processing", and a first

constituent decoder (104) that performs a "second decoding processing". A deinterleaver (114) and/or output buffer (116) provide a "memory for storing the results of the first decoding processing". Decision circuitry (118) performs a CRC check and provides an "error detector for detecting error in the results of the first decoding processing". As "results of the first decoding processing stored in said memory" are output "in accordance with the result of error detection", a "means for outputting the results ..." is evident.

Regarding claims 14 and 23, Zhang's turbo decoder (Fig. 1) can also be said to include a first constituent decoder (104) that performs a "first decoding processing", and a second constituent decoder (112) that performs a "second decoding processing". Collective decoding logic (134) provides a "decoder for executing the first and second decoding processing and executing the second decoding processing using a signal obtained by interleaving the results of the first decoding processing". A control processor (132) provides a "controller for controlling the decoder so the first decoding processing is executed and then the second decoding processing is executed".

10. Claims 15, 17, 18, 22 and 23 are rejected under 35 U.S.C. 102(a) as being anticipated by the published article "VLSI Design and Implementation of Low-Complexity Adaptive Turbo-Code Encoder and Decoder for Wireless Mobile Communication Applications" written by Hong *et al* (hereafter Hong).

Hong discloses a turbo decoder (Fig. 1b) including circuitry (Decoder1, Decoder2, Interleavers, Deinterleaver) providing a "decoder for executing first and second decoding processing". Decoder1 logic performs the "first decoding processing"

and Decoder2 logic performs the "second decoding processing". Hong also shows an "output line for outputting a signal obtained by deinterleaving the results of the second decoding processing" (data out).

Regarding claims 17, 18 and 22, Hong shows Estimator Checker logic generating a "stop iteration" signal, providing a "controller" or "selector" for outputting "one of the results of the first and second decoding processing", the "one of the results" being from a selected iteration of Decoder2.

11. Claims 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,122,763 to Pyndiah *et al* (hereafter Pyndiah).

Pyndiah shows a "turbo decoder" (Fig. 6) for a product code having row and column parities. The "turbo decoder" has a single elementary decoder (65) and a memory (67) operated as an interleaver and a deinterleaver, thereby storing "the results of the first and second decoding processing alternatively". Row decoding provides an "error detector" for column decoding, and column decoding provides an "error detector" for row decoding. The operations of either row or column decoding can be described as "first decoding processing". Decoding results are thus output from the memory "in accordance with the result of the error detection". It is here noted that the row and column decodings both involve processing both types of parities.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the published article "Illuminating the Structure of Code and Decoder of Parallel Concatenated Recursive Systematic (Turbo) Codes" written by Robertson (hereafter Robertson) in view of the published article "A Novel ARQ Technique using the Turbo Coding Principle" written by Narayanan *et al* (hereafter Narayanan).

Robertson discloses a turbo decoder (Fig. 1) including an "error detector" ("Stop iterations" generating logic) that apparently works in parallel with the operation of the turbo code constituent decoders (MAP1, MAP2) as there is no suggestion of halting the turbo code constituent decoders (MAP1, MAP2) prior to generation of the "Stop iterations" signal. There is no suggestion by Robertson of stopping decoding after a fixed number of iterations, although it was presumably clear at the time that permitting the decoding iterations to continue without end on uncorrectable data wouldn't be practical.

Narayanan discloses Turbo decoding with error detection and a preset maximum number of iterations before decoding is presumed not possible and an ARQ NACK is sent.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Robertson's turbo decoder with a control condition that limits the number of iterations, as Narayanan's turbo decoder does. Such a realization would have been obvious because it was presumably clear at the time that

permitting decoding iterations to continue without end on uncorrectable data wouldn't be practical, and because Narayanan teaches the need for such decoding effort limiting in a practical turbo decoding system.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker

Primary Examiner
Art Unit 2133

smb